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Attn: Certificate of Correction Branch U.S. Patent and Trademark Office	**571-273-8300**	

FROM: John Platt PHONE: 602-382-6367

RE: U.S. Patent No. 7,035,617

MESSAGE:

Request for Certificate of Correction (3 Pages)

Thank you.
John H. Platt

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ORIGINAL DOCUMENT: Will not be sent NUMBER OF PAGES (Including Cover): 7

CONFIRMATION NO.: CLIENT MATTER NO.: 36956.1000

PLEASE RETURN TO: Kim L. Brown 16S21 PERSONAL FAX: No

REQUESTOR: John Platt DIRECT LINE: 602-382-6367

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CERTIFICATE OF FACSIMILE PURSUANT TO 37 C.F.R. § 1.8

I hereby certify that this correspondence is being transmitted via facsimile to the United States Patent and Trademark Office at (571) 273-8300 and is addressed to: Attn: Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on:

Date: 5/30/06 By: Kim L. Brown

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT

Applicant:	Kenneth V. Buer et al.	Docket No.:	36956.1000
Patent No.:	7,035,617	Serial No.:	10/066,024
Issue Date::	April 25,2006	Filing Date:	January 29, 2002
Title:	HIGH POWER BLOCK UPCONVERTER	Confirmation No.:	2094

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. §§ 1.322

Attn: Certificate of Correction Branch
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Pursuant to 37 C.F.R. §§1.322, Patentee hereby requests a Certificate of Correction be issued to correct errors noticed in the claims. In accordance with the provisions of 37 C.F.R. §§1.322 of the Rules of Practice, approval of the attached Certificate of Correction for the above-identified patent is requested.

The errors in Claims 1, 7, 11, and 12 were made by the Office. (Compare to listing of claims in the last Response to Office Action dated October 27, 2005.) Claims 1, 7, 11, and 12, should read:

1. A block-up converter comprising:

a subharmonic mixer;

wherein said subharmonic mixer is configured to receive a first input signal,

wherein said first input signal is an intermediate frequency signal;

wherein said subharmonic mixer is further configured to receive a second input

signal, wherein said second input signal is a local oscillator signal in the Ku band or lower;

wherein said subharmonic mixer is configured to output a RF signal having a frequency greater than 26 GHz;

a filter configured to receive said RF signal and filter unwanted spurious signals which may be present in said RF signal; and

a power amplification device configured to receive said RF signal and to provide a desired signal gain;

wherein said subharmonic mixer, said filter, and said amplification device are located on a single multi-chip module, such that all signal interfaces with said multi-chip module occur at frequencies less than 26 GHz except for the final output of said RF signal from said multi-chip module;

wherein said multi-chip module is configured to be surface mounted using a lead frame interface;

wherein said block-up converter is configured to be a high power block-up converter, wherein high power is defined to be any power greater than 1 ~~Wart~~Watt; and

wherein said block-up converter is configured to provide a high frequency output, wherein high frequency is defined to be any frequency greater than 26 GHz.

7. The ~~black-up~~block-up converter of claim 6, wherein said multi-chip module is configured to be surface mounted using a lead frame interface.

11. The block-up converter of claim 6, wherein said ~~maid-chip~~multi-chip module is configured to be a drop-in component within the next higher assembly level.

12. A method for assembling a block-up converter on a single multi-chip module, the method comprising the steps of:

electrically connecting a subharmonic mixer on a multi-chip module to a filter on said multi-chip module;

wherein said subharmonic mixer is configured to receive a first input signal, wherein said first input signal is an intermediate frequency signal;

wherein said subharmonic mixer is further configured to receive a second input

signal, wherein said second input signal is a local oscillator signal in the Ku band or lower;

wherein said subharmonic mixer is configured to output a RF signal having a frequency greater than 26 GHz;

wherein said filter is configured to receive said RF signal and filter unwanted spurious signals which may be present in said RF signal; and

electrically connecting said filter to a power amplification device that is also located on said multi-chip module,

wherein said power amplification device is configured to receive said ~~RE~~RF signal and to provide a desired signal gain;

wherein said block-up converter is configured to be a high power block-up converter, wherein high power is defined to be any power greater than 1 Watt; and

wherein said block-up converter is configured to provide a high frequency output, wherein high frequency is defined to be any frequency greater than 26 GHz.

The Commissioner is hereby authorized to charge any fees which may be required for the Certificate of Correction to Deposit Account No. 19-2814. **A duplicate copy of this document is enclosed.**

If there are any questions or unresolved issues, the undersigned would welcome a telephone call to the number shown below.

Dated: May 30, 2006

Respectfully submitted,

By John H. Platt

John H. Platt
Reg. No. 47,863

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wherein said subharmonic mixer is configured to output a RF signal having a frequency greater than 26 GHz;

a filter configured to receive said RF signal and filter unwanted spurious signals which may be present in said RF signal; and

a power amplification device configured to receive said RF signal and to provide a desired signal gain;

wherein said subharmonic mixer, said filter, and said amplification device are located on a single multi-chip module, such that all signal interfaces with said multi-chip module occur at frequencies less than 26 GHz except for the final output of said RF signal from said multi-chip module;

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